4. A memory structure as recited in claim 3, wherein said buffer of each of said controllers stores at most three of said responses.

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5. A memory structure as recited in claim 3, wherein said return path has twice the bandwidth of said forward path.

6. A memory structure as recited in claim 3, wherein each of said memory units has internal logic for copying data from said each memory unit to a request therefor, thereby forming a modified request, and for forwarding said modified request to controllers on said return path.

REMARKS

Claims 1 and 2 have been rejected under 35 U.S.C. §112 as being indefinite because of the improper use of "latter". This has been corrected.

All claims have been rejected under 35 U.S.C. §103 as being unpatentable over COX.

COX describes a memory structure having serially connected link controllers 13, 15, 17, which the Examiner is reading upon the claimed controllers. The COX controllers are used to interrogate and configure the memory modules 20 during setup (see col. 4, line 39 to col. 5, line 2). These COX controllers are **not** used during routine real time memory read and write accesses by the processor. At col. 2, lines 62-65, COX specifically

states, "The MCL system 10 is used only to interrogate and configure the memory modules 20, and is not used during real time memory accesses by the host system." System controller 33 is used during real time accesses, which uses a bus system for accesses.

Claims 1-4 and 6 have been amended extensively anyway in order to place the claims in better form and to more precisely claim the algorithm used in this invention to control the return path buffers, so as to achieve the scalable memory features described in the specification. COX fails to teach or suggest this algorithm.

CONCLUSIONS

It is believed that all of the pending claims fully meet all of the requirements of 35 U.S.C. § 112 and also distinguish readily over all of the cited art, when taken individually and in combination. Accordingly, allowance of the pending claims is believed to be in order and is respectfully solicited.

Respectfully submitted,

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VERSION OF CLAIMS SHOWING CHANGES MADE

1. (AMENDED) In a memory structure having a plurality of ordered memory levels, and [a] forward and return paths for interconnecting said memory levels and a processor, each said memory level having a controller in said return path for receiving responses from an immediately higher one of said levels, if any, and for transmitting responses to an immediately lower one of said levels, except for the controller of the lowest one of said levels which transmits responses instead to said processor, each said controller having a buffer, a method of transferring requests from said processor on said forward path[s] and responses to said requests on said return path to said processor, said method comprising the steps of:

transmitting each request from said processor to each of said levels;

if a request at any one [from a memory level] of said levels is a read request addressed to the memory of [latter] said [memory] one level, then transmitting a response to [latter] said read request on said return path along with [another] up to one other response from [internal buffers] said buffer of [latter] said controller of said [memory] one level;

if a request [from a memory level] at said any one of said [memory] levels is a write request addressed to the memory of [latter] said [memory] one level, then transmitting up to two responses from said buffer of said controller [internal buffers] of [latter] said [memory] one level on said return path;

if a request [from a memory level] at said any one of said [memory] levels is [targeted] addressed to one of said levels [a] higher than said one [memory level of said memory] level, then transmitting up to two responses from [internal buffers] said buffer of said controller of [latter] said one [memory] level on said return path; and

if a request [from a memory level] at said any one of said [memory] levels is [targeted] addressed to one of said levels [a] lower than said one [memory level of said memory] level, then transmitting up to one response from [internal buffers] said buffer of said controller of [latter] said one [memory] level on said return path.

2. (AMENDED) A method as recited in claim 1, wherein at most three responses are stored in said [internal] buffer of said controller of any of said memory levels.

3. (AMENDED) A memory structure for receiving requests to and transmitting responses from a memory in said structure, [respectively,] said structure comprising:

an ordered set of memory levels, each memory level having a controller and a memory unit, [which] said memory unit [is] being a portion of said memory;

a forward path for transmitting said requests to said memory levels [, starting from lower of said levels and proceeding to a higher of said levels]; and

a return path for transmitting responses to said requests from any [higher] one of said levels which is higher than an immediately [to] lower one of said levels to said immediately lower level;[,]

wherein [each] said controller [at each] of said one [memory] level transmits responses to said requests on said return path [from each level] to a buffer in said controller [at a] of said immediately lower level in accordance with the following algorithm:

a. if a request at said [any] one [of said levels] level is a read request addressed to said one level, then transmitting a [first] response to [latter] said read request on said return path, along with [a second] up to one response from [internal buffers] said buffer of said controller of said one level, to [buffers in a] said buffer of said controller of [a] said immediately [memory level which is] lower [than said one] level,

b. if a request at said any one of said levels is a write request addressed to said one level, then transmitting no response to said write request on said return path and up to two responses from [internal buffers] said buffer of said controller of said one level on said return path to [buffers in a] said buffer of said controller of [a] said immediately [memory level which is] lower [than said one] level,

c. if a request at said any one of said levels is [targeted] addressed to one of said levels [a] higher than [of] said one [levels] level, then transmitting up to

two responses from [internal buffers] said buffer of said controller of said one level on said return path to [buffers in a] said buffer of said controller of [a memory level which is] said immediately lower [than said one] level, and

d. if a request at said any one of said levels is [targeted] addressed to one of said levels [a] lower than [of] said one [levels] level, then transmitting up to one response [to a request] from [internal buffers] said buffer of said controller of said one level on said return path to [buffers in a] said buffer of said controller of [a memory level which is] said immediately lower [than said one] level.

4. (AMENDED) A memory structure as recited in claim 3, wherein said buffer of each of said controllers [on said return path has buffers for storing] stores at most three of said responses.

5. A memory structure as recited in claim 3, wherein said return path has twice the bandwidth of said forward path.

6. (AMENDED) A memory structure as recited in claim 3, wherein each of said memory units has internal logic
for copying data [between one of] from said each memory [units] unit [and] to a request [as specified therein] therefor, thereby forming a modified request, and for forwarding said [one] modified request to controllers on said return path.